

A VHDL Library for *MTM/BST* Communication

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Motivation

- To build a library of VHDL models for an 1149.1 board-level test controller , including a P1149.5 interface layer, with the aim of enabling the development of an MTM/BST system-level test strategy

Requirements

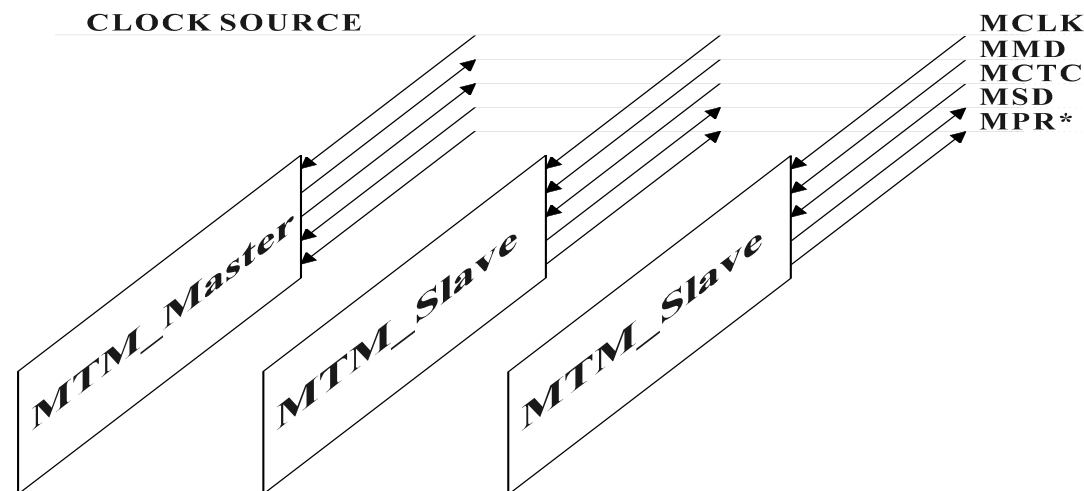
- **The system-level test specification should be an open ended specification allowing user-defined functionality**
- **Reusability of proven models**
 - board-level test controller
 - board-level ATPG tool
- **Flexible implementation accommodating changes in the system-level test specification**

Outline of the presentation

- **The IEEE 1149.1 and P1149.5 Standards**
- **The test protocol**
- **The board-level test controller**
- **The VHDL library**
- **Future directions**
- **Conclusions**

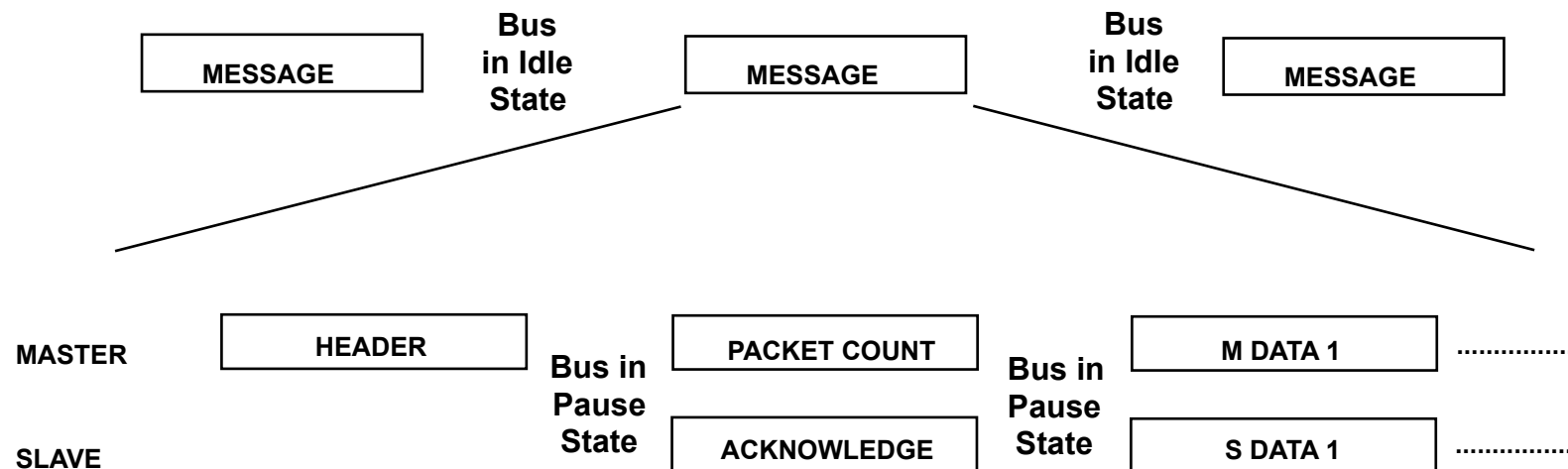
The P1149.5 Module Test and Maintenance (MTM) - Bus

- The IEEE P1149.5 MTM - Bus defines a serial backplane bus, linking a Master-module and up to 250 Slave-modules. The MTM Bus is formed by 5 dedicated signals: MTM Clock (MCLK), MTM Control (MCTL), MTM Master Data (MMD), MTM Slave Data (MSD) and the optional MTM Pause Request (MPR)



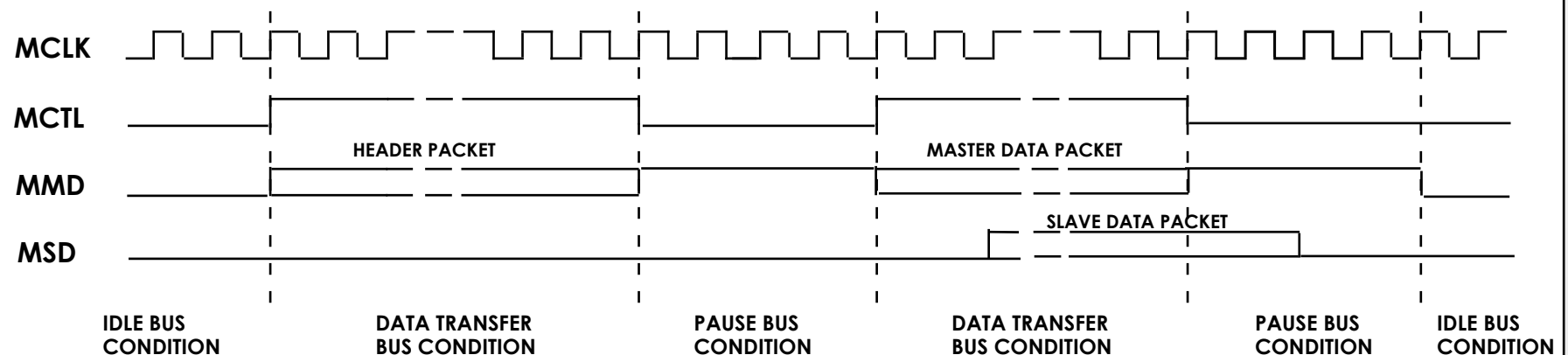
The P1149.5 Module Test and Maintenance (MTM) - Bus

- Message exchanging between the M-module and S-modules is based on a packet transfer protocol. Packets are delimited by Bus Pause conditions and messages are delimited by Bus Idle conditions



The P1149.5 Module Test and Maintenance (MTM) - Bus

- State transitions of the Master Link Layer State Machine (LLSM) and of the Slaves LLSMs are controlled by MCTL and MMD. The MSD line may also be used to signal an interrupt to the Master during a Pause or Idle Bus condition. The MPR line may be used by the Slave to extend the Bus Pause condition



Boundary Scan Test: The IEEE 1149.1 Std.

- The IEEE 1149.1 Std. defines a standard boundary scan architecture and test access port

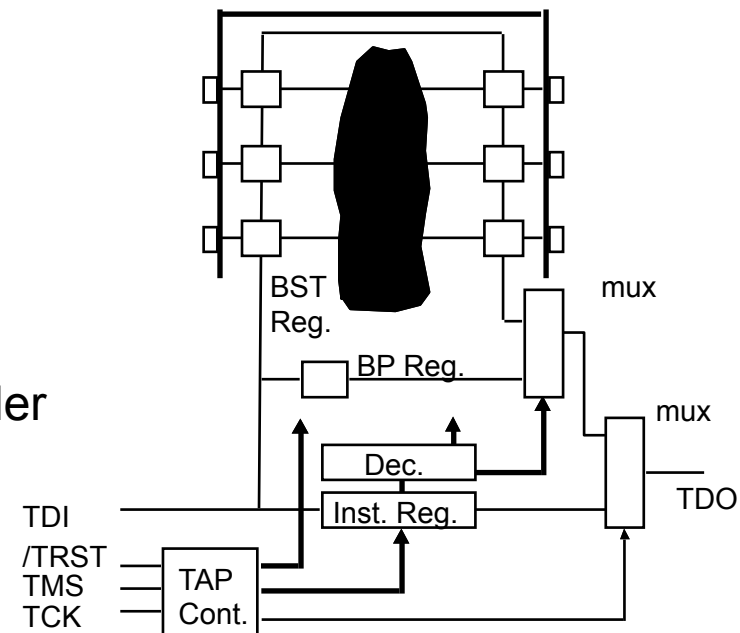
Inst. Reg.: Instruction Register

BP Reg.: Bypass Register

Dec.: Instruction decoder

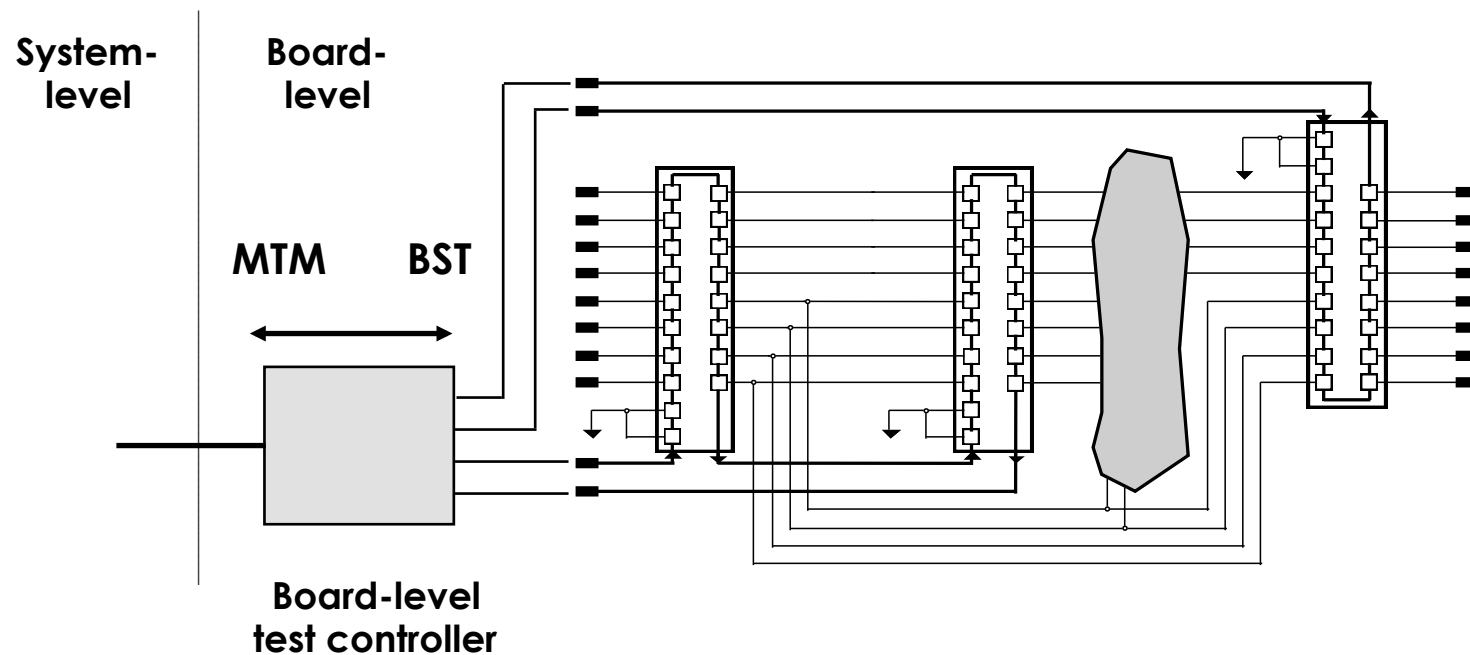
BS Reg.: Boundary Scan Register

TAP Cont.: Test Access Port Controller



Boundary Scan Test: The IEEE 1149.1 Std.

- Keywords: Board-level, structural, digital



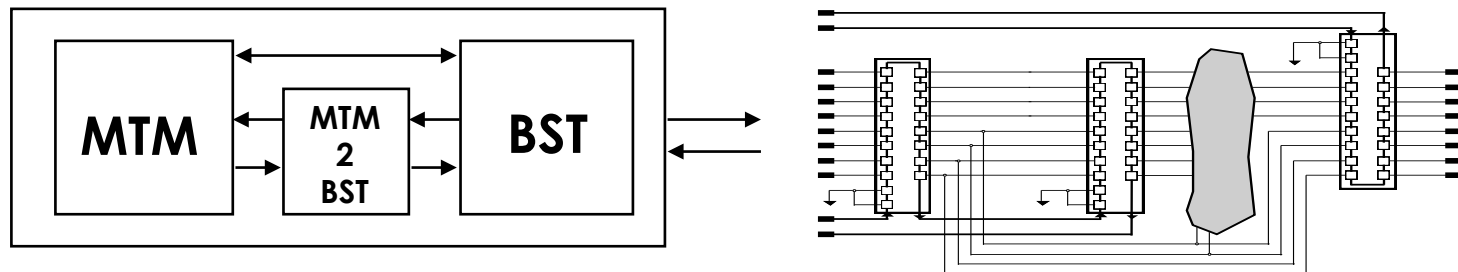
The test protocol

- The Board-level test program for a given S-module is transmitted through the *MTM - Bus*:
 - A Header containing the Slave address and the *RUN_PROC* command
 - A *PACKET COUNT* packet indicating the length of the test program
 - A set of *DATA PACKETS* containing the test program
- Fault detection will set an error flag in the board-level test controller and generate an interrupt to the *MTM - Bus Master*



The board-level test controller

- The board-level test controller contains:
 - The MTM interface layer
 - The BST controller
 - The MTM2BST Linker Block



The Board-level test controller

The board-level test controller

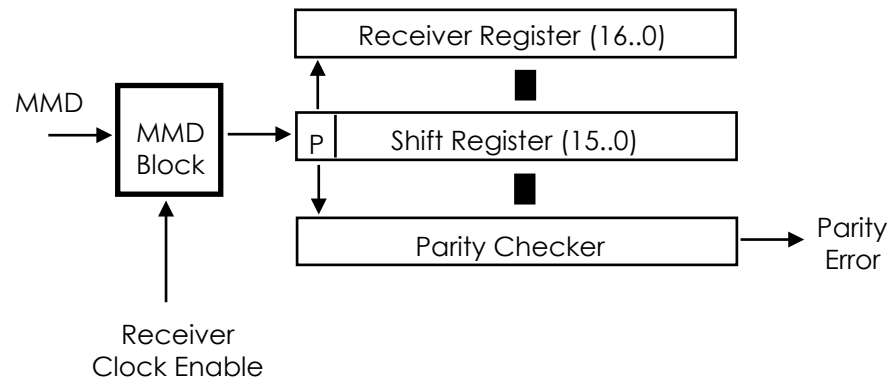
The MTM interface layer

- **The MTM interface layer is sub-divided into the following blocks:**
 - **Sender and Receiver blocks**
 - **Address Compare block**
 - **Slave Link Layer Controller**
 - **Slave Status Registers**
 - **Instruction decode and execution control unit**

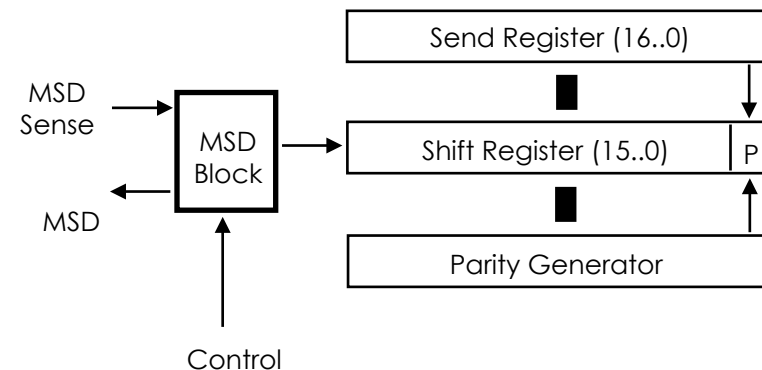
The board-level test controller

The MTM interface layer

- The sender and receiver blocks are responsible for the serial exchange of data through the MSD/MMD lines (16-bit packets with odd parity)



Receiver block diagram

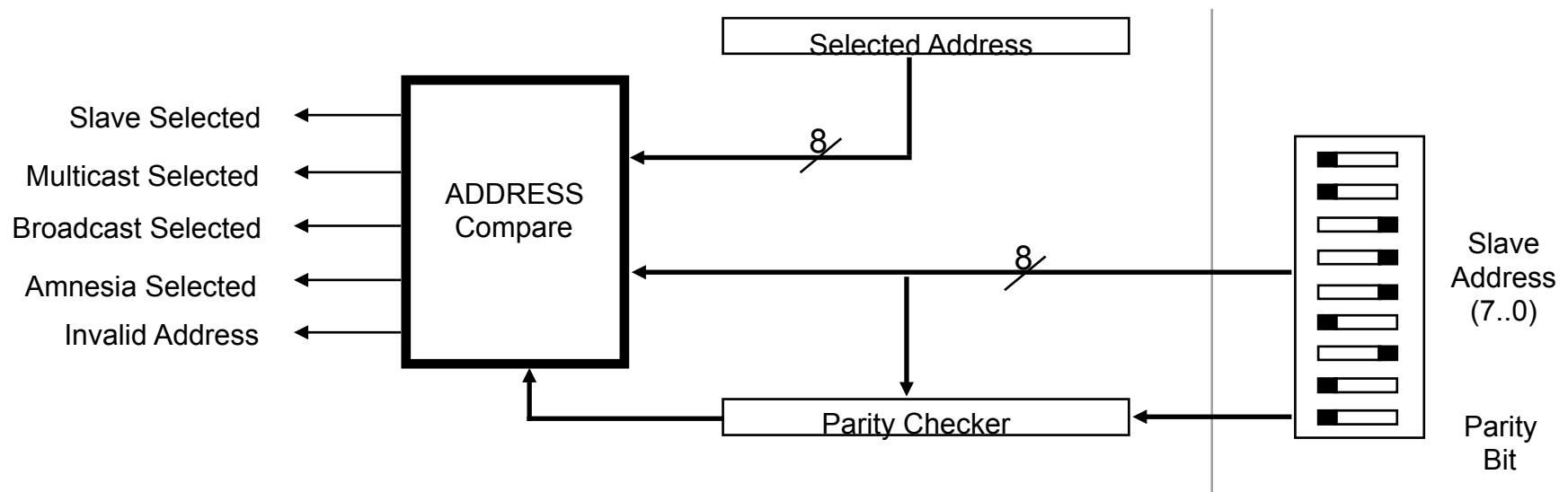


Sender block diagram

The board-level test controller

The MTM interface layer

- The address compare block decodes the Header address field



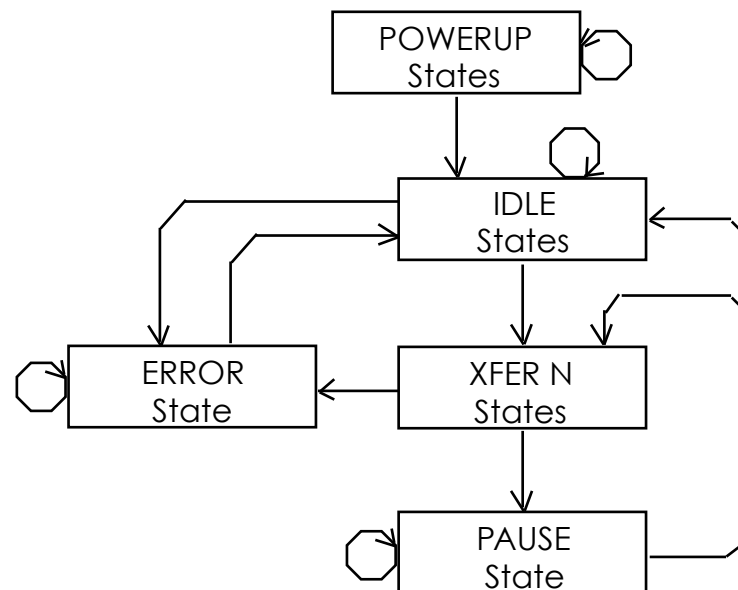
Block diagram of the address compare block

The board-level test controller

The MTM interface layer

- The Slave Link Layer State Machine is responsible for keeping the S-Module synchronised with the Bus activity. It includes five main groups of states:

- Power-up
- Idle
- Transfer
- Pause
- Error



The board-level test controller

The MTM interface layer

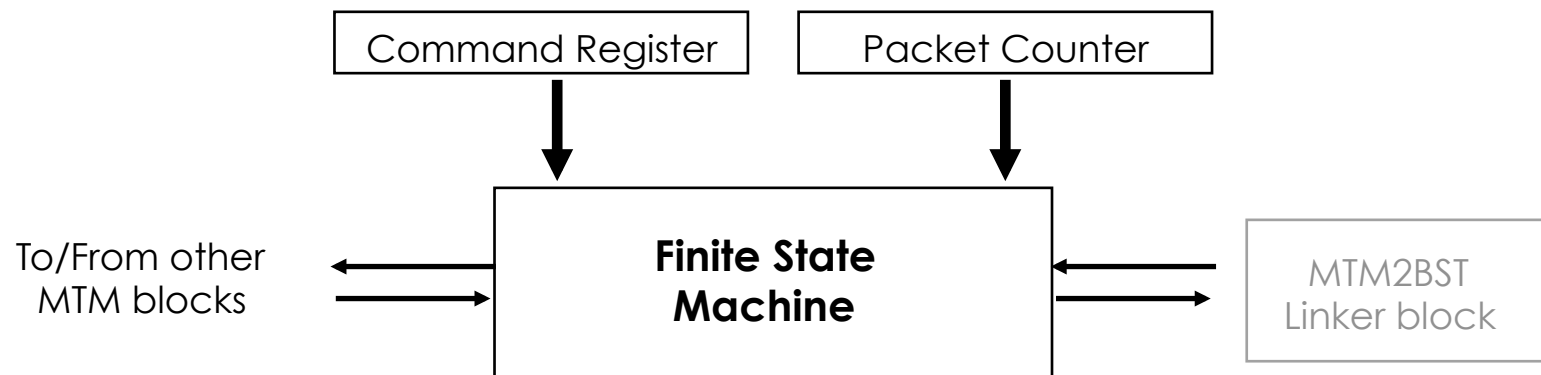
- **The Slave Status Registers store information about the system activity and errors that may have occurred. All these registers can be read by the Master**

SLAVE STATUS REGISTER	General Status Condition of MTM - Slave. The BSE and EVO bits, when set, require an interrupt.
BUS ERROR REGISTER	Reports several Bus error conditions. The logical OR of some bits drives the BSE bit of the Slave Status Register.
MODULE STATUS REGISTER	Module Specific Status that may set the EVO bit - (recommended; presently not implemented).
USER-DEFINED STATUS REGISTER	Additional Status registers that may set the EVO bit of the Slave Status Register.

The board-level test controller

The MTM interface layer

- The instruction decode and execution control unit links all MTM blocks



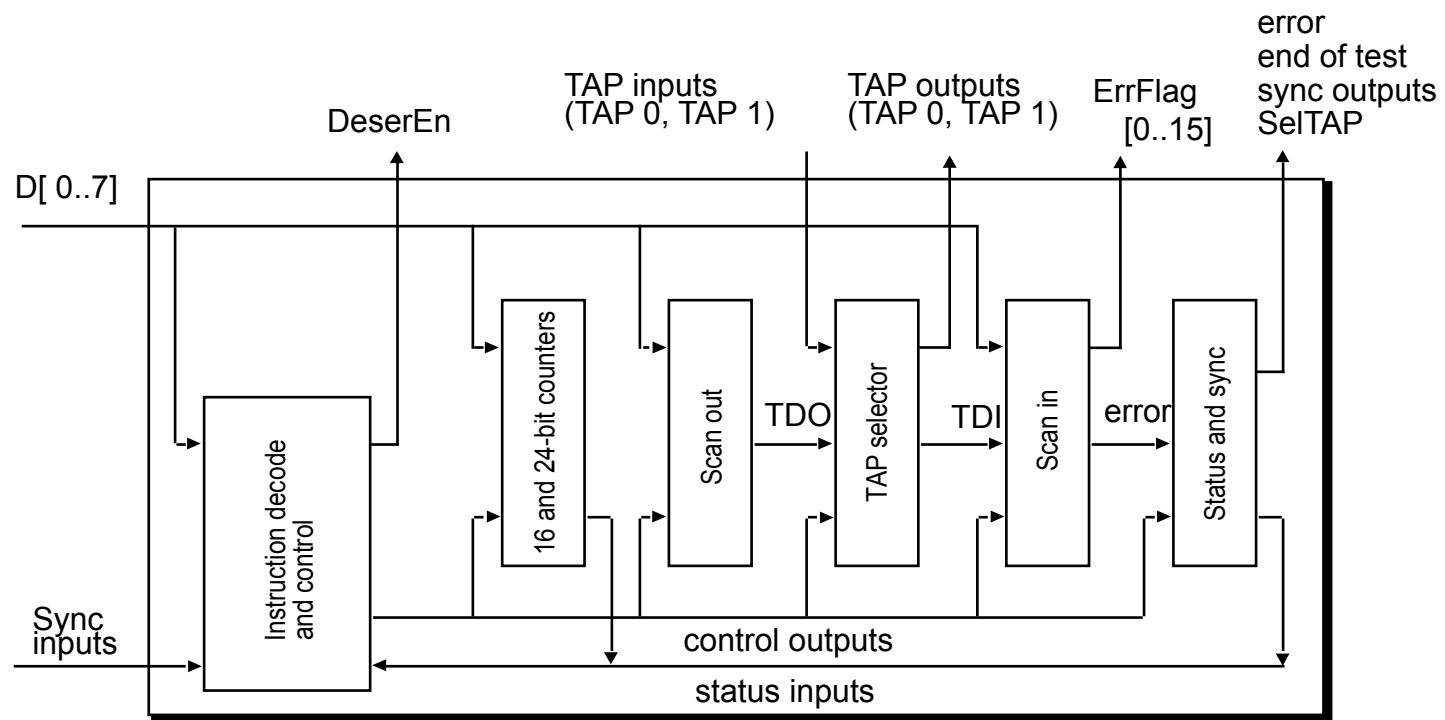
The board-level test controller

The BST controller

- **The BST controller is a fourth generation dedicated processor core able to control two board-level scan chains**
- **It's instruction set maps the low-level operations required to control the board-level BST infrastructure**

The board-level test controller

The BST controller



Block diagram of the BST controller

The board-level test controller

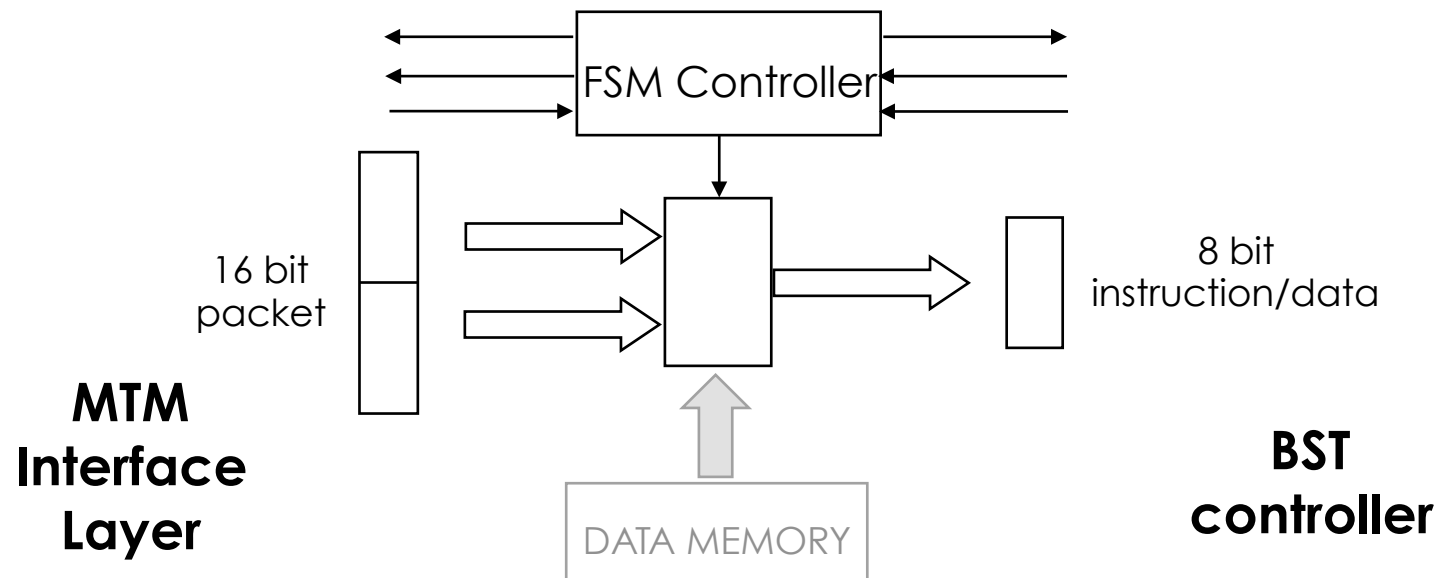
The BST controller

Command class	Operation description	Command name
control of BST infrastructure	Apply a '0' pulse to TRST line	TRST
	Apply a test clock pulse while holding TMS at a given value 'X'	TMS0, TMS1
	Shift out vector, no comparison	NSHF
	Shift out vector, comparing with expected values	NSHFCP
	Apply N test clock pulses, while holding TMS at '0'	NTCK
	Select active TAP	SELTAP0, SELTAP1
control of the synchronism protocol	Set synchronism output to a given value 'X'	SSA0, SSA1, SSB0, SSB1
	Wait for synchronism input to be at a given value 'X'	WSA0, WSA1, WSB0, WSB1
control of internal resources	Load internal counter (16 or 24 bits long) with N	LD C16,N LD C24,N
	Select internal error flag (15..0)	SERFLAG N
	Stop test program execution	HALT

The instruction set of the BST controller

The board-level test controller

The MTM2BST Linker Block



Block diagram of the MTM2BST Linker Block

The VHDL library

- **The VHDL library contains a set of functional models leading to a modular architecture based on the three main blocks described:**
 - The MTM interface layer
 - The BST controller
 - The MTM2BST Linker block
- **This library allows customised solutions**
- **The VHDL models were successfully simulated using the MINT software from the Swedish Institute for Microelectronics**

Future directions

- **Synthesis**
- **Local test program memory**
- **MTM/BST system-level test strategy**
- **Diagnostic resolution**

Conclusion

- **The work presented described a library of VHDL models developed to enable a *MTM/BST* system-level strategy**
- **Reusability and flexibility are two key attributes of the proposed implementation**
- **Approval of the P1149.5 by the IEEE Standards Board will create the required conditions to fully exploit a *MTM/BST* (test) infrastructure**